

(P.G.)
MPHY CC-121 (Sem. III)

Dr. Sanjay Kumar
Assistant Professor

Dept. of Physics
JSS Jain College,

K.S.U, H.R.

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Different Combination of the Basic Logic Gates

The OR, AND and NOT gates are the three basic circuits that make up all digital circuits.

(i) NAND gate:



(ii)

| Inputs | | Output |
|--------|---|------------------|
| A | B | AND (Y) NAND (Y) |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

(iii)



(iii)
Fig. 1

NAND gate is a combination of AND and NOT gates. Output of NAND gate is NOT gate. It is connected to the output of a NOT gate. If in a NAND gate, the output of a NOT gate is opposite to the output of an AND gate. This is clear from the truth table for the NAND gate. The truth table for NAND gate is developed by inverting the outputs of the AND gate.

The NAND function is $Y = A \cdot B$. The output from a NAND gate is always 1 except when all the inputs are 1. P(ii) shows the logic symbols for a NAND gate. The little bubble (small circle) on the right end of the symbol means an inverter. The symbol means logic buffer. The output of NAND gate is $Y = A \cdot B$.

(i)

| Inputs | Output |
|--------|-----------------|
| A B | OR (Y) NAND (Y) |
| 0 0 | 1 |
| 1 0 | 1 |
| 0 1 | 1 |
| 1 1 | 0 |

(ii)

(iii)

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It is a combination of OR gate and NOT gate. In other words, output of OR gate is connected to the input of a NOT gate as shown in Fig. 2.1. The output of OR gate is inverted to form NOR gate. From truth table for NOR gate has been developed by inverting the outputs of the OR gate.

The Boolean expression for NOR gate is

$$Y = \overline{A+B}$$

The output from a NOR gate is high (1) only when all the inputs are low (0). If any of the inputs is high (1) the output is low (0). Fig. 2.1(ii) shows the logic symbol for a NOR gate. The bubble (small circle) at the output indicates inversion.